# MINIATURIZED MULTISTAGE POWER AMPLIFIERS FOR THE 10.95- TO 12.75-GHz COMMUNICATIONS SATELLITE BAND*

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## Abstract

This paper describes the design and performance of three prototype power amplifiers that use a combination of MMICs and "quasi-monolithic" circuits, and which are intended for use in a satellite multibeam phased-array antenna. The amplifiers are designed to maximize DC-to-RF conversion efficiency and linearity while satisfying additional requirements for output power and minimum size. The four-stage, 30-dB gain modules deliver an output power of 2 W at 2-dB compression, with an efficiency of 25 percent and a two-tone, carrier-to-third-order intermodulation distortion ($C/I_3$) level of 16 dB.

## INTRODUCTION

In order to reduce earth station costs, and thereby allow the wider use of satellite communications, earth stations must become smaller and simpler. To maintain the same quality of service as the stations become smaller, the required effective isotropic radiated power (e.i.r.p.) of the satellite-based transmitter must be increased. This can be accomplished by increasing the total radiated power, which will require more prime power, or by increasing the gain of the antenna (*i.e.*, generating a number of narrow "pencil" beams). The added capability to reconfigure (change the shape and/or location of) these beams and to change relative beam powers would allow the dynamic reallocation of resources. Both of these benefits can be realized by using an active phased-array antenna in which solid-state power amplifiers (SSPAs) at each radiating element simultaneously amplify all the signals across the full bandwidth of the array.

The requirements of the SSPAs in an active phased-array antenna are significantly different from those of the high power amplifiers (HPAs) used in current satellites. For example, the HPAs in existing satellites typically operate over the bandwidth of a single, relatively narrow bandwidth transponder and amplify a single carrier or a small number of carriers. In contrast, the SSPAs in the active antenna must operate over the entire satellite down-link band and simultaneously amplify many more carriers.

Thus SSPAs for active phased-array antennas must satisfy several, often conflicting, requirements. First, to minimize intermodulation distortion arising from multicarrier operation, the SSPA must be as linear as possible. Second, to reduce the DC power requirements for the array and to lower the field-effect transistor (FET) operating temperature (thereby increasing SSPA reliability), the SSPA must be efficient. However, high linearity and high efficiency are conflicting requirements because, as the SSPA is operated closer to saturation, its efficiency increases while its linearity degrades. Third, the SSPAs must operate over the full system bandwidth, rather than the narrow bandwidth of the individual transponders. Finally, to minimize the mass of the array and to allow the radiating elements to be tightly packed, SSPA size and mass must be minimized.

This paper describes the design, fabrication, and RF performance of three four-stage gallium arsenide (GaAs) FET power amplifiers which serve as prototypes for SSPAs that will be incorporated into a transmit phased-array antenna for the 12-GHz satellite band. To obtain the optimum combination of linearity and efficiency, the output stages of the SSPA are operated in class AB mode and contain low-impedance terminations at the second harmonic. To satisfy size and bandwidth requirements, the SSPA utilizes fully monolithic and quasi-monolithic circuitry and employs the technique of partial matching in the output stages to allow broadband operation.



Three SSPAs were built and tested. The four-stage, 30-dB gain modules deliver a single-tone output power of 2 W at 2-dB compression ($P_{in}$ = 5 dBm), with a single-tone efficiency of 25 percent and a two-tone carrier-to-third-order intermodulation distortion ($C/I_3$) of 16 dB. When backed off ($P_{in}$ = 3 dBm) to achieve a 20-dB $C/I_3$ level, the single-tone output power is 1.6 W, with a corresponding single-tone efficiency of 21 percent. In comparison, a traveling wave tube amplifier (TWTA) operated at a $C/I_3$ level of 16 dB exhibits a single-tone efficiency of about

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35 percent; at a $C/I_3$ level of 20 dB, the TWTA single-tone efficiency is about 22 percent. In a typical conventional system, however, at least 2 dB of loss is incurred in the RF power distribution network following the TWTA, thus reducing the overall efficiency by about 40 percent.

## DESIGN

Figure 1 is a block diagram of the SSPA, giving the performance of each stage. The low-power input stages are fully monolithic, while the higher power output stages use the quasi-monolithic approach (*i.e.*, monolithic passive matching circuits with discrete chip FETs) described in Reference 1. In addition, the output stages are operated in a balanced configuration, which results in a low-output voltage standing-wave ratio (VSWR) for the complete SSPA. The designs for the various stages are based on FET models derived from small-signal and large-signal measurements.

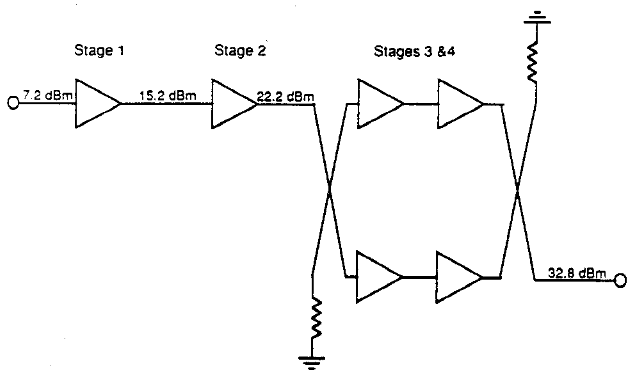


*Figure 1. Ku-Band SSPA Block Diagram*

Stages 1 and 2 contain identical monolithic microwave integrated circuit (MMIC) chips (fabricated on 0.090-mm-thick GaAs) which are designed for low distortion in order to minimize their contribution to the distortion introduced by the complete SSPA. Because the output power required from the first stage is low, this chip is operated at a low drain voltage (5 V). The second stage must deliver medium power (20 dBm), so this chip is operated at a slightly higher drain voltage (7 V). Since these stages are also designed to consume low DC power compared to the output stages, they do not appreciably affect the overall SSPA efficiency.

The design and operation of the output stages greatly influence the linearity, efficiency, and bandwidth of the complete SSPA. To obtain the required characteristics, the output stages of the SSPA employ the following:

- class AB operation of the fourth stage
- FETs preselected for high gate-to-drain breakdown voltage and low pinchoff voltage
- low-reactance termination of the second harmonic
- partial matching of the fourth-stage FETs
- use of quasi-monolithic circuits on thicker substrates to minimize circuit losses.

To obtain the best combination of efficiency and linearity, the last stage is operated in class AB mode, which causes even harmonics to be generated. The low-impedance second harmonic termination performs wave-shaping of the drain voltage, which increases the available drain voltage swing at the fundamental frequency, thereby increasing the amplifier efficiency.

The input impedance of the typical 1-W device used in the output stage is about 1 Ω at 12 GHz. The physical realization of a network which raises this impedance level to a reasonable value (35 to 50 Ω) across a 15-percent bandwidth is difficult, and the circuit losses associated with such a network are high.

To overcome the difficulties involved in matching the input of a wide FET over a broad bandwidth at 12 GHz, the technique of partial matching is employed. In this approach, simple matching circuits are used to raise the impedance level of three smaller gate-width (higher impedance) FETs. The inputs of the partially matched devices are combined at a higher impedance level and then transformed to the 35- to 50-Ω range. To reduce losses, power-combining is done directly at the drains of the output stage FETs.

## RESULTS

Three four-stage units were built and tested. Figure 2 is a photograph of the amplifier, which measures 1.25 x 3.75 cm. Figure 3 shows the amplifier mounted in one of the radiating elements of the phased-array antenna.

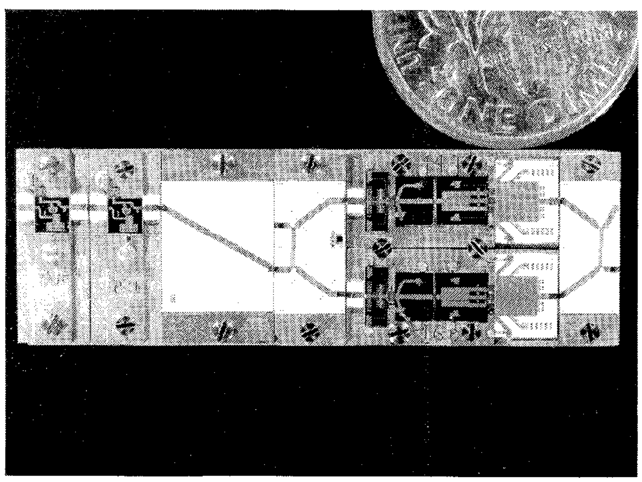

*Figure 2. Ku-Band SSPA Assembly*

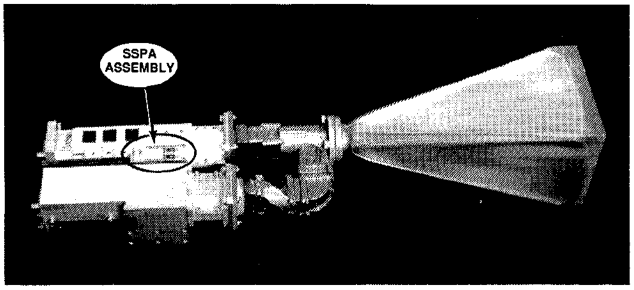


*Figure 3. Active Antenna Radiating Element (indicating location of SSPA assembly)*

Figure 4 depicts the small-signal gains for the three modules. Although designed for the full 10.95- to 12.75-GHz band, the units were optimized for best large-signal performance over the 11.7- to 12.7-GHz band. Over this band, unit 1 has a gain of 28.5 ± 0.5 dB; unit 2 has gain of 29.5 ± 0.3 dB; and unit 3 has gain of 28.5 ± 0.5 dB. No gain-trimming was done on these units.

Figure 5 contains plots of total two-tone output power and $C/I_3$ vs input power for each SSPA operating at 12.2 GHz ($F_1$ = 12.20 GHz and $F_2$ = 12.21 GHz). With the input drive level set at 0 dBm per tone (+3 dBm, total), SSPA 1 has a $C/I_3$ of 20 dB; SSPA 2 has a $C/I_3$ of 20 dB; and SSPA 3 has a $C/I_3$ of 19 dB. As Figure 6 shows, the two-tone performance for SSPA 2 is nearly constant across the 11.7- to 12.7-GHz band.

Figure 7 contains plots of output power and efficiency for the three units under single-tone operation at 12.2 GHz. With the input drive level at 3 dBm, the power-added efficiency for all three units is 21 percent. The output power levels at this drive level are 32, 32.5, and 32.0 dBm for SSPAs 1, 2, and 3, respectively. At saturation, the SSPA output power and efficiency are 33.5 dBm and 28 percent,

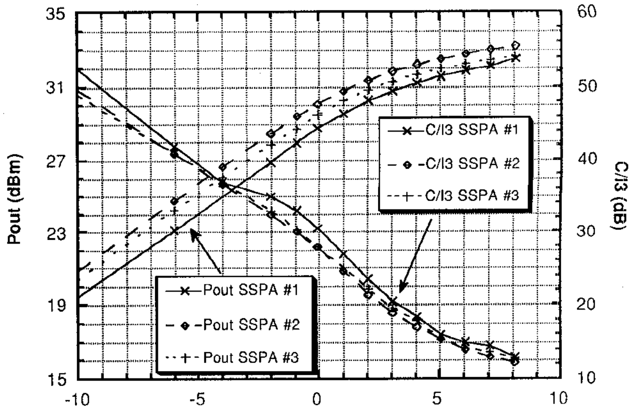


*Figure 5. Two-Tone Output Power and $C/I_3$ vs Two-Tone Input Power at 12.2 GHz for Three SSPAs*

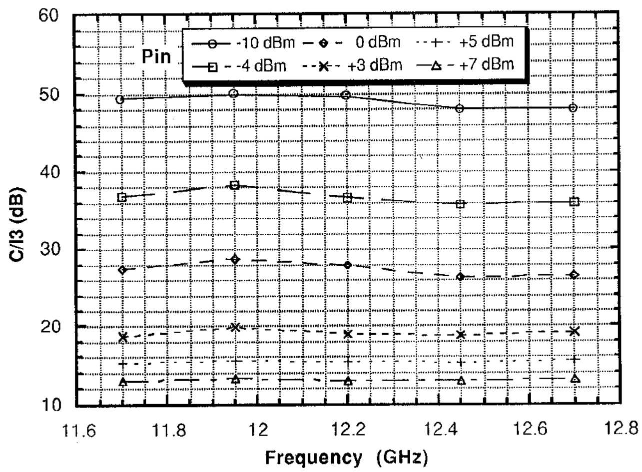


*Figure 6. $C/I_3$ as a Function of Input Power vs Frequency for SSPA 2*

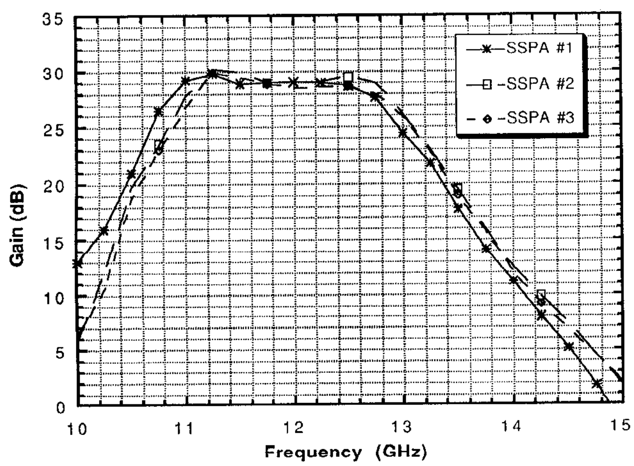


*Figure 4. Small-Signal Gain vs Frequency for Three SSPAs*

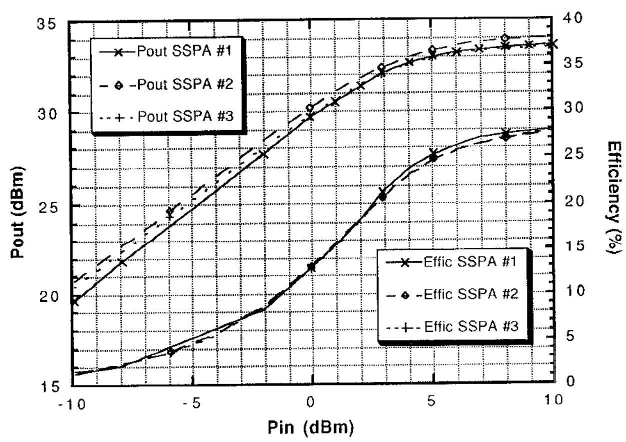


*Figure 7. Single-Tone Output Power and Efficiency vs Input Power at 12.2 GHz for Three SSPAs*

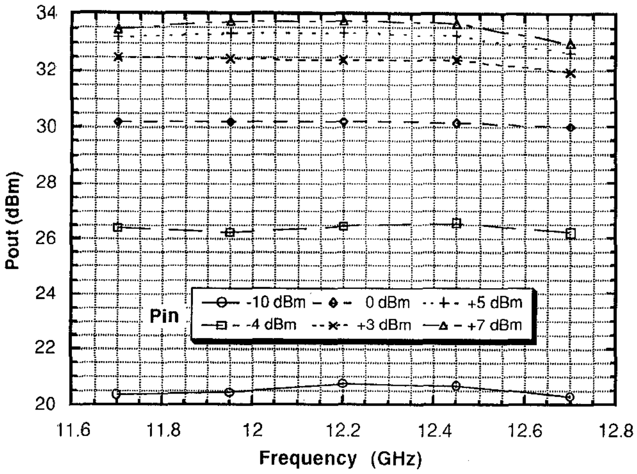


*Figure 8. Output Power as a Function of Input Power vs Frequency for SSPA 2*

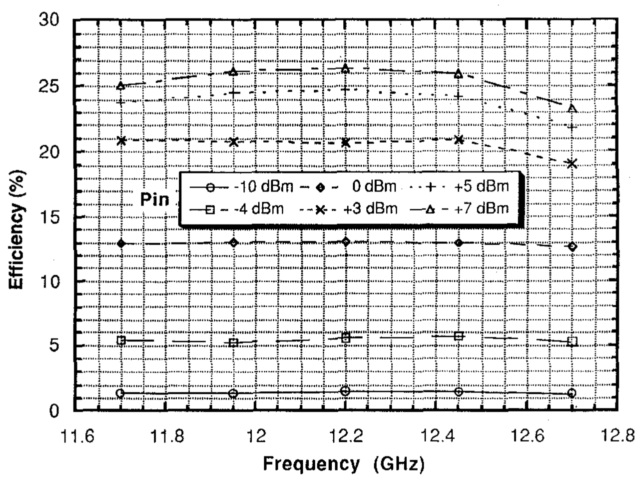


*Figure 9. Efficiency as a Function of Input Power vs Frequency for SSPA 2*

respectively. Figures 8 and 9 show that, for SSPA 2, the output power and efficiency are nearly invariant across the 11.7- to 12.7-GHz band.

## CONCLUSIONS

The design and performance of three prototype power amplifiers that use a combination of MMICs and quasi-monolithic circuits, and which are intended for use in a satellite multibeam phased-array antenna, have been described. The amplifiers were designed to maximize DC-to-RF conversion efficiency and linearity while satisfying additional requirements for output power and minimum size. The output stages are operated in a class AB mode and utilize a low-impedance second harmonic termination and partial matching to achieve broad bandwidth. The low-power stages employ fully monolithic circuitry. The four-stage, 30-dB gain modules deliver an output power of 2 W at 2-dB compression, with an efficiency of 25 percent and a two-tone $C/I_3$ of 16 dB.

## ACKNOWLEDGMENTS


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## REFERENCES


(1) B. D. Geller and P. Goettle, "Quasi-Monolithic 4-GHz Power Amplifiers With 65-percent Power-Added Efficiency," IEEE-MTT-S International Microwave Symposium, New York, New York, May 1988, *Digest*, pp. 835–838.